ACTEL / MICROSEMI

FPGA Type	Maximum *'clk'* Frequency	Logic Modules (CORE)
ProASIC3 (A3P400 144FBGA I Std)	50 MHz (MII; RMII)	1947
IGLOO (AGL400V5 144FBGA I Std)	50 MHz (MII; RMII)	2019
IGLOO2 (M2GL010T 484FBGA I Std)	125 MHz (GMII)	SEQUENTIAL (R-cells): 583 COMB (C-cells): 995
Fusion (AFS600 484FBGA I -1)	50 MHz (MII; RMII)	2040
Axcelerator (RTAX250S 208CQFP Mil Std)	50 MHz (MII; RMII)	SEQUENTIAL (R-cells): 685 COMB (C-cells): 1163

Note: The number of used logic modules is an approximation, since the tools do not provide detailed information of the resources used in a "per module" basis.

ALTERA

FPGA Type	Maximum 'clk' Frequency	Flip-Flops	ALUTs	ALMs	Logic Cells
MAX II (EPM2210FF324I5)	50 MHz (MII;RMII)	512	-	-	982
Cyclone III (EP3C5E144I7)	125 MHz (GMII)	514	-	-	1091
Cyclone IV (EP4CE22F17I7)	125 MHz (GMII)	513	-	-	1066
Stratix II (EP2S60F484I4)	125 MHz (GMII)	512	591	563	-

Note: MAX II compiled with MII options ('g_MDC_DIVIDER' = 10, 'g_MII_DATA_LENGTH' = 4)

XILINX

FPGA Type	Maximum 'clk' Frequency	Flip-Flops	4-LUTs	Slices	Macrocells
CoolRunnerII (XC2C128-6-TQ144)	NA	NA	-	-	NA
Spartan3 (XC3S1000-5FG320)	TX*: 100 MHz (MII) RX: 125 MHz (GMII)	527	1007	677	-
Spartan6 (XC6SLX45-3FGG484)	125 MHz (GMII)	527	619	271	-
Virtex4 (XC4VLX15-12SF363)	125 MHz (GMII)	526	940	643	-
Zync (XC7Z010-3CLG400)	125 MHz (GMII)	516	502	303	-

Note *: The Transmitter needs further optimizations during synthesis and P&R.